

1 TRANSFER MODE; U.S. Patent Application No. 09/964,315 TI-
2 31779); filed on even date herewith; invented by Shakuntala
3 Anjanaiah and Natarajan Seshan; and assigned to the
4 assignee of the present application: APPARATUS AND METHOD
5 FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN A HOST
6 PROCESSING AND A MULTI-TARGET DIGITAL SIGNAL PROCESSING IN
7 AN ASYNCHRONOUS TRANSFER MODE; U.S. Patent Application No.
8 09/964,158; filed on even date herewith; invented by Martin
9 Li, Jay Reimer Shakuntala Anjanaiah, Natarajan Seshan and
10 Patrick Smith; and assigned to the assignee of the present
11 application: and APPARATUS AND METHOD FOR INPUT CLOCK
12 SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE
13 UNIT; U.S. Patent Application No. (Attorney Docket No.
14 09/964,164; filed on even date herewith; invented by
15 Shakuntala Anjanaiah; and assigned to the assignee of the
16 present application are related applications.

17

18 **Please delete the Paragraph beginning on page 3, line 4 and**
19 **replace this Paragraph with the following Paragraph.**

20

21 "The asynchronous transfer mode interface unit is only
22 one of the possible devices that can provide an interface
23 between a digital signal processing unit and other data
24 processing devices. Another interface device is the I/O
25 interface device. In fabricating a chip, the device can
26 include one type of interface unit or both types of
27 interface units. The inclusion of only one type of
28 interface unit limits the utility of the chip. The
29 inclusion of both types of interface units on a chip

1 increases the both the size and the complexity of the
2 chip."

3

4 **Please delete the Paragraph beginning on page 13, line 30**
5 **and replace this Paragraph with the following Paragraph.**

6

7 "Referring to Fig. 13, the operation of the (transmit)
8 EVENT signal is illustrated. After initialization of the
9 transmit portion of the UTOPIA interface unit in step 1300
10 or as part of the continuing operation of the interface
11 unit, a determination is made in step 1301 whether a space
12 for the storage of a complete data cell is available in the
13 transmit buffer memory unit. When the determination is
14 yes, then in step 1302 a transmit EVENT signal is applied
15 to the direct memory access unit. In response to the
16 generation of the EVENT signal, a data cell is transmitted
17 through the direct memory access unit to the buffer memory
18 storage unit in step 1303. In step 1304, as soon as the
19 transfer of the data cell has begun and the first word of
20 the cell is written, the EVENT signal is cleared. Note
21 that the EVENT signal is reasserted as soon as the first
22 word is written and the buffer memory unit has space
23 available. The immediate assertion of the EVENT signal
24 improves the interface unit throughput. The process then
25 returned then returns to step 1301 to determine whether
space in the transmit buffer memory unit is available for
storage of an entire data cell. When the determination is
in step 1301 is negative, the process returns to step 1301
and continues to cycle until space is available for the
storage of an entire data cell.

1 Please delete the Paragraph beginning on page 16, line 21
2 and replace this Paragraph with the following Paragraph.

3

4 "The foregoing description has described the interface
5 unit as including a buffer memory unit. In the preferred
6 embodiment, the buffer memory unit is implemented by a
7 first-in/first-out memory unit. The memory unit is
8 provided with the capacity to store two data cells. The
9 communication bus causes the signals to be exchanged
10 between the master unit and the slave unit to have a
11 relatively slow clock speed. Because of the relatively
12 slow clock speed of the communication bus, the filling or
13 emptying of the buffer memory in the direction of the
14 communication will be much slower than the filling and the
15 emptying of the buffer memory unit in the direction of the
16 direct memory access unit. Similarly, although the direct
17 memory access unit can handle only one data transfer at a
18 time, because of the difference in clock speed between the
19 communication bus and the processing unit of which the
20 direct memory access unit is part accommodated by the
21 interface unit.

22

23

24 In the Claims

25

26 Please amend Claim 1 as follows.

27

28 1. (Currently Amended) An interface unit controlling
29 the exchange of signals between a data processing unit and
30 a communication bus, the data processing unit including a